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10/588,415	07/14/2008	Karlheinz Freywald	LEO 009 PA	8357

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2818	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,415	FREYWALD, KARLHEINZ	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/4/06,7/14/08,10/2/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-11, 13-19 are pending in the Application.

Election/ Restriction

2. Applicant's election of claims 1-11 pertains to Species I for prosecution **with traverse** in the communication with the Office on June 14th 2010 is acknowledged. The traversal is on the ground that the search for all species will not be a burden for the Office because they are related with each other..

The Examiner respectfully disagrees. As discussed in the previous Office Action, there is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

The Requirement is still deemed proper and therefore is made **FINAL.**

Nevertheless, upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

. Furthermore, applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 is indefinite because of recitation of the limitation -- " polysilicon layer "-- lacks antecedent basis , there is no -- " polysilicon layer "--recited in claim 2 and claim 1 that claim 5 depends on.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes

of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Baba et al. (U.S. Patent 5,126,817) thereafter Baba 817 listed in Applicant IDS..

With regard to claim 1, Baba 817 discloses (the abstract, fig 4, fig 5) a method of forming at least one, dielectrically insulating isolation trench, for the dielectric isolation of regions of different potential, in particular, of device structures formed above an SOI wafer including an active semiconductor layer, by forming at least one void in said at least one isolation trench, thereafter forming a hermetically tight seal of the at least one void with respect to the semiconductor wafer surface, the method comprising: performing a first fill step in the form of a controlled deposition, adapted to trench geometry, to thereby form oxide layers (layer 27 in fig 4) , at trench walls, said oxide layers having an increasing thickness (fig 4,fig 5, combined element 27) towards upper trench edges and forming a first bottleneck (fig 4,fig 5,the bottle neck is the bottle neck formed by the top portion of void element 26 interface with layer 27 in fig 4)

7. Claim 1,11 is rejected under 35 U.S.C. 102(b) as being anticipated by Begley et al. (U.S. Patent 5,933,746) thereafter Begley 746

With regard to claim 1, Begley 746 discloses (the abstract, fig 1A,fig 2A) a method of forming at least one, dielectrically insulating isolation trench, for the dielectric isolation of regions of different potential, in particular, of device structures formed above an SOI wafer (fig

1A,fig 2A, layer 14 is an oxide , with active layer are silicon ,column 1 lines 1-40, column 2 lines 29-40,therefore the wafer disclosed by Begley 746 is a SOI or silicon-on-insulator wafer) including an active semiconductor layer, by forming at least one void in said at least one isolation trench, thereafter forming a hermetically tight seal of the at least one void (fig 2A, void 36,column 3 lines 5-16) with respect to the semiconductor wafer surface, the method comprising: performing a first fill step in the form of a controlled deposition, adapted to trench geometry, to thereby form oxide layers (layer 20 fig 1A) , at trench walls, said oxide layers having an increasing thickness towards upper trench edges and forming a first bottleneck (fig 1A.fig 2A)

With regard to claim 11, Begley 746 discloses (the abstract, fig 1A,fig 2A) a method wherein a surface of the sealed trench is planarized. (fig 2A,fig 3A,column 3 lines 25-30)

Claim Rejections - 35 USC § 103

8. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US patent 6,791,155) thereafter Lo 155 listed in Applicant IDS..

With regard to claim 1, Lo 155 (the abstract, fig 1,fig 2,fig 3)all the invention of a method of forming at least one, dielectrically insulating isolation trench, for the dielectric isolation of regions of different potential, in particular, of device structures formed above an wafer including an active semiconductor layer, by forming at least one void in said at least one isolation trench, thereafter forming a hermetically tight seal of the at least one void with respect to the semiconductor wafer surface, the method comprising: performing a first fill step in the form of a controlled deposition, adapted to trench geometry, to thereby form oxide layers, at trench walls, said oxide layers having an increasing thickness (fig 2,fig 3 element 130), due to the round slope of the trench) towards upper trench edges and forming a first bottleneck (fig 2,fig 3 the bottleneck at the interface of element 120,130 in fig 2)

Not disclosed in Lo 155 is the limitation wherein the wafer is a SOI (silicon-on-insulator) wafer. The Examiner, however, takes official notice that this limitation is obvious because the used of Silicon-on-insulator is known in the art at the time the invention was made.

A person skilled in the art at the time the invention was made would have been motivated to incorporate a silicon-on-insulator substrate in Lo 155 method because Silicon-on-insulator is known in the art to improve the isolation between devices and enhanced devices performance such as operating speed and therefore increase the chance of the Lo 155 method to achieve commercial success.

10. Claim 8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba et al. (U.S. Patent 5,126,817) thereafter Baba 817 listed in Applicant IDS.

With regard to claim 8, as set forth in the rejection of claim 1, Baba 817 discloses all the

Invention except for the limitation wherein said SOI wafer comprises micro electronic mechanic systems (MEMS) in a semiconductor layer formed on the oxide layer.

The Examiner, however, takes official notice that this limitation is obvious because the incorporation of the MEMS device in the semiconductor formed on the Oxide layer (i.e. SOI or Silicon-on-insulator substrate) similar to the substrate disclosed by Baba 817 is known by a person of ordinary skill in the art at the time the invention was made

Moreover, a person skilled in the art at the time the invention was made would have been motivated to incorporate this feature in order to increase the marketability of the Baba 817 invention and make it a commercial success.

With regard to claim 9, as set forth in the rejection of claim 1, Baba 817 discloses all the invention except for the limitation wherein the at least one trench has a high aspect ratio, preferably higher than 15:1. This limitation, however, is considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).***

11. Claim 2-4,6-7, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US patent 6,791,155) thereafter Lo 155 in view of Marty et al. (U.S. patent 6,828,646) thereafter Marty 646.

With regard to claim 2, as set forth in the rejection of claim 1, Lo 155 discloses all the invention except for the limitation wherein the method further comprising subsequently anisotropically RIE etching the oxide in a first step until the oxide layers, s are removed from the wafer surface and subsequently continuing the RIE etching process in a second step for removing the oxide layer in an upper trench portion to a defined depth a later sealing portion of the at least one_void displacing downwardly the first bottleneck to form a further bottleneck Marty 646, however, discloses a method wherein the method further comprising (the abstract,fig 3C,3D,3E) subsequently etching the oxide in a first step until the oxide layers, s are removed from the wafer surface and subsequently continuing etching process in a second step for removing the oxide layer in an upper trench portion to a defined depth a later sealing portion of the at least one void displacing downwardly the first bottleneck to form a further bottleneck (fig 3C,3D)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features , as taught by Marty 646, into the Method disclosed by Lo 155 and come up with an intermediate method named Lo 155 in view of Marty 646

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to provide the Lo 155 method with an isolation trench structure with low coupling capacitance but does not induced high mechanical stress to the substrate , taught by Marty 646 , column 1 lines 50-57) in order to improve the Lo 155 method and makes it a commercial success.

Furthermore, as set forth above, the combined Lo155 in view of Marty 646 method disclosed all the invention of claim 2 except for the use of anisotropic RIE etching.

This limitation, however, is considered obvious because Marty 646 nevertheless discloses the use of dry etching including RIE etching (column 4 lines 50-67) and anisotropic RIE etching is an obvious variant of RIE or dry etching.

Moreover, note that a person skilled in the art at the time the invention was made would have been motivated to use all the available method at his disposal to achieve the desired result..

With regard to claim 3, the combined Lo 155 in view of Marty 646 will disclosed a method , further comprising second oxide deposition, performed by a low pressure CVD process, (Lo 155 fig 3 layer 140) thereby again depositing an oxide near a step formed by the further bottleneck to seal -the at least one void located there below, said second oxide deposition being stopped when the sealed portion of the oxide layer above said at least one void is grown above a wafer level of the semiconductor layer .(Lo 155 fig 3.)

With regard to claim 4, Lo 155 discloses a method wherein after sealing said trench, the wafer surface is planarized and a technological process sequence is continued. (Lo 155 column 4 lines 35-52)

With regard to claim 6, Lo 155 disclosed a process wherein the same process technique is used during the first and the second depositions. (Lo 155 column 3 lines 45-67)

With regard to claim 7, Marty 646 disclosed a method wherein different process techniques are used during the first and the second deposition (Marty 646, column 5 lines 15-67,column 6 lines 1-10)

With regard to claim 10, Lo 155 discloses a method wherein the formed sealed of the at least one void is located below the level of the surface of the active semiconductor layer (Lo 155 fig 3, Void 145 is below the active layer surface of layer 100)

12. Claim 2, 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Begley et al. . (US patent 5,933,476) thereafter Begley 476 in view of Gaw et al. (US patent 6,303,464) thereafter Gaw 464.

With regard to claim 2, as set forth in the rejection of claim 1, Begley 476 discloses all the invention including deposition of a polysilicon layer (fig 2A,polysilicon 34, column 3 lines 25-42) except for the limitation wherein the method further comprising subsequently anisotropically RIE etching the oxide in a first step until the oxide layers are removed from the wafer surface and subsequently continuing the RIE etching process in a second step for removing the oxide layer in an upper trench portion to a defined depth a later sealing portion of the at least one void displacing downwardly the first bottleneck to form a further bottleneck Gaw 464,

however, discloses a method wherein the method further comprising (the abstract,fig 2,fig 3) subsequently etching the oxide in a first step until the oxide layers, are removed from the wafer surface and subsequently continuing etching process in a second step for removing the oxide layer in an upper trench portion to a defined depth a later sealing portion of the at least one void displacing downwardly the first bottleneck to form a further bottleneck (fig 3C,3D)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features , as taught by Gaw 464, into the Method disclosed by Begley 746 and come up with an intermediate method named Gaw 464 in view of Begley 746

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to provide the Begley 746 method with an isolation trench structure with low coupling capacitance , mechanically strong and stable , cost-effective to implement and other advantages , taught by Gaw 464 (column 2 lines 8-32) in order to improve the Begley 746 method and makes it a commercial success.

Furthermore, as set forth above, the combined Begley 746 in view of Gaw 464 method disclosed all the invention of claim 2 except for the use of anisotropic RIE etching.

This limitation, however, is considered obvious because anisotropic RIE etching.is known in the art at the time the invention was made .moreover, anisotropic RIE etching is known in the art as an effective method to achieved the desired structural results

With regard to claim 5, to expedite the prosecution of the case, the Examiner assumes that the Applicant will correct the deficiencies of claim 5 to make it in compliance with 35

U.S.C. 112 second paragraph and will examine the claim as best as the Examiner can understand it.

Therefore, with regard to claim 5, as set forth in the rejection of claim 2, the combined Begley 746 in view of Gaw 464 disclose all the invention except for the limitation wherein RIE etching of the first trench filling in the area outside said trench stops on a polysilicon layer

This limitation, however, is considered obvious since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954) .

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

14. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

15. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6:30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T. Nguyen/

Primary Examiner
Art Unit 2818